

HINTS & SOLUTIONS**TOPIC : SOLID & SEMICONDUCTOR DEVICES****EXERCISE # 1****SECTION (A)**

1. N-type semiconductors are neutral because neutral atoms are added during doping.
2. In insulators, the forbidden energy gap is very large, in case of semiconductor it is moderate and in conductors the energy is 0 eV.
16. Value of forbidden energy gap in semiconductor is 1 eV.
17. GaAs is an alloy semiconductor.
19. Holes are found in p-type semiconductor.
20. In semiconductor, no covalent bond breaks at 0 K, so, no electron is free at 0 K. At room temperature some covalent bonds break, so, some electrons and holes become free. More covalent bonds break at high temperature and so, number of free electrons increases at high temperature.
22. Increase of temperature increases resistance of conductor but decreases resistance of semiconductor.
24. Cu is conductor and Ge is semiconductor.
Increase of temperature increases resistance of conductor but decreases resistance of semiconductor.
26. In a p-type semiconductor, the germanium is doped with elements which have incomplete outer shell of electrons like aluminium, boron and gallium.
27. Presence of large number of free electrons in metallic bond solids, make them good conductor of electricity.
28. The donor level is found only in n-type semiconductor. The donor level lies closely below the bottom of the conduction band.
30. The difference in the variation of resistance with temperature in metal and semiconductor is caused due to difference in the variation of the number of charge carriers with temperature.
36. In the given situation the number of holes in valence band is greater than number of electrons in conduction band. So it is p-type semiconductor.
39. $I = n_e A v_d$

$$\frac{I_e}{I_h} = \frac{n_e \times (v_d)_e}{n_h \times (v_d)_h}$$

$$\text{Here, } \frac{n_e}{n_h} = \frac{7}{5}, \frac{I_e}{I_h} = \frac{7}{4}$$

$$\frac{7}{4} = \frac{7}{5} \times \frac{(v_d)_e}{(v_d)_h} \Rightarrow \frac{(v_d)_e}{(v_d)_h} = \frac{5}{7} \times \frac{7}{4} = \frac{5}{4}$$
40. If lattice constant of semiconductor is decreased, then E_c and E_v decrease but E_g increases.

Solids & Semiconductor Devices

46. Covalent bonding exists in semi-conductor.

SECTION (B)

26. By using $E = \frac{V}{d} = \frac{0.6}{10^{-6}} = 6 \times 10^5 \text{ V/m}$
 27. The diode is in reverse biasing so current through it is zero.

28. Current flow is possible and $i = \frac{V}{R} = \frac{(4-1)}{300} = 10^{-2} \text{ A}$

29. For full wave rectifier $\eta = \frac{81.2}{1 + \frac{r_f}{R_L}} \Rightarrow \eta_{\max} = 81.2\% \quad (r_f \ll R_L)$

36. The emitter base junction is forward biased while collector base junction is reversed biased.

47. ac  dc

48. In a p-n junction diode, majority carriers are holes on p-side and electrons on n-side. Holes, thus diffuse to n-side and electrons to p-side. Thus diffusion causes an excess positive charge in the n-region and an excess negative charge in the p-region and an excess negative charge in the p-region near the junction. Thus double layer of charge creates an electric field which exerts a force on the electrons and holes, against their diffusion. Thus electric field becomes strong enough as diffusion proceeds to stop it. In the equilibrium position, there is a barrier, for charge motion with the n-side at a higher potential than the p-side.

The junction region has a very low density of either p or n-type carriers, because of inter diffusion. It is called depletion region. There is a barrier V_B associated with it. This is the potential barrier.

49. When the connection of battery is reversed, then a semiconductor device is reverse biased. We know that in forward biasing of p-n junction the current is of the order of milliampere while in reverse biasing the current is of the order of microampere (negligible). Thus, device is a p-n junction.

65. When p-side of p-n junction is given more positive voltage as compared to n-side, then junction diode becomes forward biased.

66. In reverse biasing, the applied voltage V on the n-side is positive and is negative on the p-side. The applied bias V and the barrier potential V_B are in the same direction making the effective junction potential $V + V_B$. As a result, the junction width will increase. The higher junction potential restricts the flow of majority carriers. So, reverse bias current will be due to the minority carriers only.

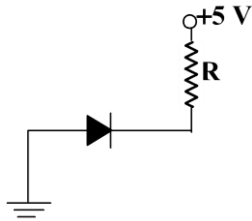
67. Due to reverse biasing the width of depletion region increases and current flowing through the diode is almost zero. In the case electric field is almost zero at the middle of the depletion region.

72. p-n photodiode is a semiconductor diode that produces a significant current when illuminated. It is reverse biased but is operated below the breakdown voltage.

Energy of radiation = band gap energy

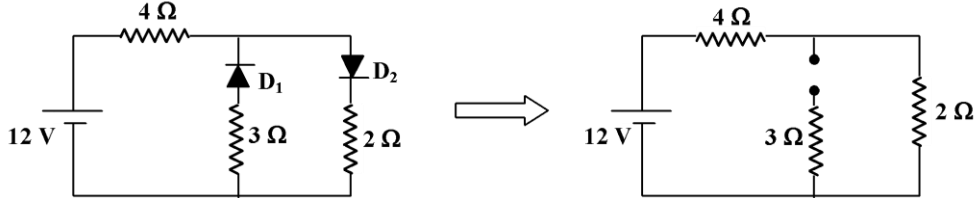
ie, $h\nu = 2.0 \text{ eV}$

$$\text{or } \nu = \frac{2.0 \times 1.6 \times 10^{-19}}{6.6 \times 10^{-34}} \approx 5 \times 10^{14} \text{ Hz}$$



75.

This circuit compels the diode to be reverse-biased.
 \therefore (2) is correct.



76.

$$i = \frac{12}{6} = 2 \text{ amp} \therefore (4) \text{ is correct.}$$

77.

Diode is forward-biased in the first half cycle and the amplitude of the signal is 5V.



Correct choice: (4)

83.

For a wide range of values of load resistance, the current in the Zener diode may change but the voltage across it remains unaffected. Thus the output voltage across the Zener diode is a regulated voltage.

86.

Diode is reverse-biased so current through A_1 is zero.

87.

The term LED is abbreviated as 'Light Emitting Diode'. It is a forward-biased p-n junction which emits spontaneous radiation. Current in the circuit = 10 mA = 10×10^{-3} A and voltage in the circuit = $6 - 2 = 4$ V. From Ohm's law,

$$\therefore R = \frac{V}{I} = \frac{4}{10 \times 10^{-3}} = 400 \Omega$$

SECTION (C)

3.

α is the ratio of collector current and emitter current while β is the ratio of collector current and base current.

4.

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.98}{1 - 0.98} = 49$$

5.

In common emitter configuration of a transistor, the input current is a base current. Input current

$$i_B = \frac{\Delta V_B}{R_B} = \frac{0.01}{1000} = 10^{-5} \text{ A}$$

Also current gain

$$\beta = \frac{i_c}{i_B}$$

$$\therefore i_c = \beta i_B = 50 \times 10^{-5} \text{ A}$$

$$= 500 \times 10^{-6} \text{ A} = 500 \mu\text{A}$$

$$10. \quad \beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$$

$$\beta = \frac{I_C}{I_B} \Rightarrow I_C = \beta I_B = 49 \times 0.02 \text{ mA} = 0.98 \text{ mA}$$

$$V_{\text{Load}} = I_C R_L = (0.98 \text{ mA}) [5K\Omega] = 4.9 \text{ volt}$$

11. To switch on the transistor, the emitter - base junction of a transistor is forward biased while collector - base junction is reverse biased. The cut - off voltage for silicon is 1V, so to switch on a silicon transistor a potential difference of 1V approximately is required between the base and emitter.

$$12. \quad \beta = \frac{I_C}{I_B} \quad I_B = \frac{I_C}{\beta}$$

$$I_B = \frac{5 \text{ mA}}{100} = 5 \times 10^{-5} \text{ A} \quad I_C = \frac{10 - V_{CE}}{1 \text{ k}\Omega} = 5 \text{ mA} \quad R_B = \frac{10 - V_{CE}}{I_B} = \frac{10 - 0}{5 \times 10^{-5}} = 2 \times 10^5 \Omega$$

13. Power gain = current gain x voltage gain

$$\text{Voltage gain} = \beta \frac{R_{\text{out}}}{R_{\text{in}}} = \beta \frac{5}{2} \times 50$$

$$\text{So, Power gain} = 50 \times 50 \times \frac{5}{2} = \frac{12500}{2} = 6250$$

16. AC power gain is ratio of change in output power to the change in input power.
AC power gain

$$= \frac{\text{Change in output power}}{\text{Change in input power}} = \frac{\Delta V_c \times \Delta i_c}{\Delta V_i \times \Delta i_b} = \left(\frac{\Delta V_c}{\Delta V_i} \right) \times \left(\frac{\Delta i_c}{\Delta i_b} \right) = A_v \times \beta_{AC} \times \frac{200}{100}$$

$$\therefore \beta_{AC} = 25$$

$$\text{Now, AC power gain} = A_v \times \beta_{AC} = 50 \times 25 = 1250$$

17. When NPN transistor is used as an amplifier, majority charge carrier electrons of N-type emitter move from emitter to base and then base to collector.

$$19. \quad \beta = \frac{I_C}{I_B} \text{ and } I_E = I_C + I_B \quad \therefore \beta = \frac{I_C}{I_E - I_C} = \frac{5.488}{5.60 - 5.488} = 49.$$

21. The circuit arrangement is shown in figure. Collector current,

$$I_C = \frac{\text{Voltage drop across } R_L}{R_L} = \frac{1}{1000} = 10^{-3} \text{ amp}$$

$$\text{Now } V_{CE} = 9 - 1 = 8 \text{ volt}$$

$$\text{Current gain } \beta = \frac{I_C}{I_B} \quad \text{or} \quad \frac{25}{26} = \frac{10^{-3}}{I_B}$$

$$\therefore I_B = 1.04 \times 10^{-3} \text{ amp}$$

$$\text{Voltage gain} = \beta \frac{R_L}{R_C}$$

$$= \frac{25}{26} \times \frac{1000}{200} = \frac{125}{26}$$

$$\text{Power gain} = \beta^2 \frac{R_L}{R_C} = \left(\frac{25}{26}\right)^2 \times \frac{1000}{200} = \left(\frac{25}{26}\right)^2 \times 5 = 4.6$$

$$\text{Again } I_E = I_B + I_C = 1.04 \times 10^{-3} + 10^{-3} = 2.04 \times 10^{-3} \text{ A}$$

$$22. \quad A_V = \beta \frac{R_{out}}{R_{in}} \Rightarrow G = 25 \frac{R_{out}}{R_1} \quad \dots\dots\dots(i)$$

$$G_m = \frac{\beta}{R_1} \Rightarrow R_1 = \frac{\beta}{G_m} = \frac{25}{0.03}$$

$$G = 25 \frac{R_{out}}{25} \times 0.03 \quad \dots\dots(i)$$

$$G' = 20 \frac{R_{out}}{20} \times 0.02 \quad \dots\dots(ii)$$

$$G' = \frac{2}{3} G$$

$$23. \quad \text{Voltage gain} = \frac{V_{out}}{V_{in}} = \frac{I_{out}}{I_{in}} \times \frac{R_{out}}{R_{in}}$$

$$= \frac{2 \times 10^{-3}}{40 \times 10^{-6}} \times \frac{4 \times 10^3}{100} = 2 \times 1000 = 2000$$

$$24. \quad V_{CE} = 12 \text{ volt}$$

$$\frac{i_c}{i_b} = 100$$

$$\beta = \frac{i_c}{i_b}$$

$$i_c = 100 \times 0.04 \times 10^{-3}$$

$$V_{CC} = V_{CE} + I_C R_C$$

$$20 = 12 + 4 \times 10^{-3} \times R_C$$

$$R = 2 \text{ k}\Omega$$

25 By definition, the A-C current gain β is given by

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}$$

$$\therefore \Delta I_C = \beta \times \Delta I_B = 19 \times 0.4 \text{ mA} = 7.6 \text{ mA.}$$

The emitter - current is the sum of the base- current and the collector-current ($i_E = i_B + i_C$)

$$\therefore \Delta I_E = \Delta I_B + \Delta I_C = 0.4 \text{ mA} + 7.6 \text{ mA} = 8 \text{ mA.}$$

SECTION (D)

1. For 'XNOR' gate $Y = \overline{A}\overline{B} + AB$

$$\text{i.e., } \overline{0.0} + 00 = 1.1 + 0.0 = 1 + 0 = 1$$

$$\overline{0.1} + 0.1 = 1.0 + 0.1 = 0 + 0 = 0$$

$$\overline{1.0} + 1.0 = 0.1 + 1.0 = 0 + 0 = 0$$

$$\overline{1.1} + 1.1 = 0.0 + 1.1 = 0 + 1 = 1$$

2. The output D for the given combination

$$D = \overline{(A+B)}.C = \overline{(A+B)} + \overline{C}$$

If $A = B = C = 0$ then $D = \overline{(0+0)} + \overline{0} = \overline{0} + \overline{0} = 1 + 1 = 1$

If $A = B = 1, C = 0$ then $D = \overline{(1+1)} + \overline{0} = \overline{1} + \overline{0} = 0 + 1 = 1$

3. $\alpha = \frac{i_c}{i_e} = 0.96$ and $i_e = 7.2 \text{ mA}$
 $\Rightarrow i_c = 0.96 \times i_e = 0.96 \times 7.2 = 6.91 \text{ mA}$
 $\therefore i_e = i_c + i_b \Rightarrow 7.2 = 6.91 + i_b = 0.29 \text{ mA}$

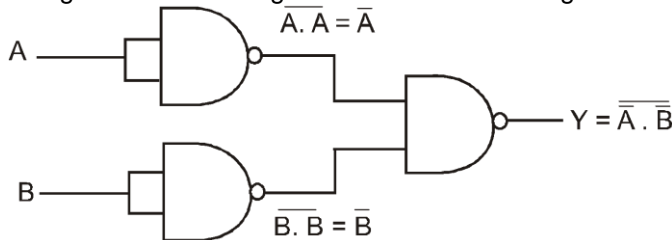
4. $i_c = \frac{90}{100} \times i_e \Rightarrow 10 = 0.9 \times i_e = 11 \text{ mA}$
 Also $i_e = i_b + i_c \Rightarrow i_b = 11 - 10 = 1 \text{ mA}$

5. $\beta = 50, R_i = 1000 \Omega, V_i = 0.01 \text{ V}$
 $\beta = \frac{i_c}{i_b}$ and $i_b = \frac{V_i}{R_i} = \frac{0.01}{10^3} = 10^{-5} \text{ A}$
 Hence $i_c = 50 \times 10^{-5} \text{ A} = 500 \mu\text{A}$

6. $\alpha = \frac{\beta}{1+\beta} = \frac{99}{1+99} = 0.99$

10. NAND gate.

13. The gates used in the given circuits are NAND gates.

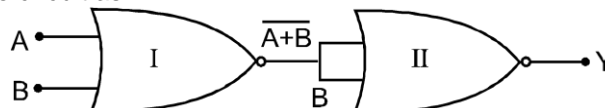


The simplified form of circuit is shown in figure.

$$\therefore Y = \overline{\overline{A} \cdot \overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} = A + B$$

Hence, this circuit works as OR gate.

15. **Key Idea:** Gates-I and II are NOR gates.
 We can simplify the gate circuit as



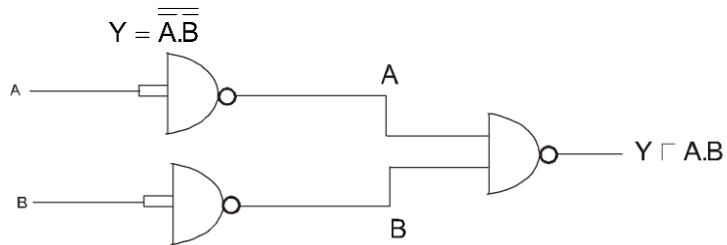
Here, gates-I and II are NOR gates. The output $(A + B)$ of gate-I will be appeared as input of gate-II. The final output is

$$Y = A + B = A + B$$

This is the Boolean expression of OR gate whose truth table is given below :

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

16. From the logic gate circuit,



By De Morgan's theorem

$$\overline{\overline{A} \cdot \overline{B}} = \overline{\overline{A}} + \overline{\overline{B}}$$

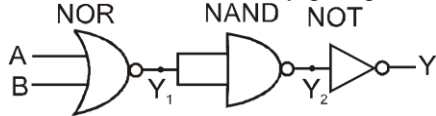
So, $Y = A + B$

or $Y = A + B$

This is Boolean expression of OR gate whose truth table is given below:

Input		output
A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

17. The gate circuit can be shown by giving two inputs A and B.



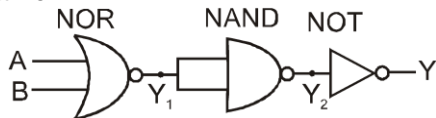
Output of NOR gate, $Y_1 = \overline{A+B}$

Output of NAND gate, $Y_2 = \overline{Y_1 \cdot Y_1}$
 $= \overline{Y_1 + Y_1}$
 $= \overline{\overline{A+B} + \overline{A+B}}$
 $= (A+B) + (A+B)$
 $= A+B$

Output of NOT gate, $Y = \overline{Y_2}$
 $= \overline{A+B}$

which is the output of NOR gate.

Alternative :



NOR			NAND		NOT	
A	B	Y ₁	Y ₁	Y ₁	Y ₂	Y
0	0	1	1	1	0	1
0	1	0	0	0	1	0
1	0	0	0	0	1	0
1	1	0	0	0	1	0

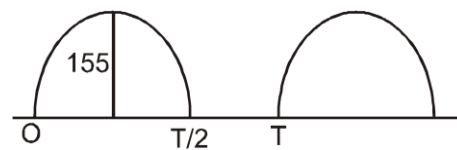
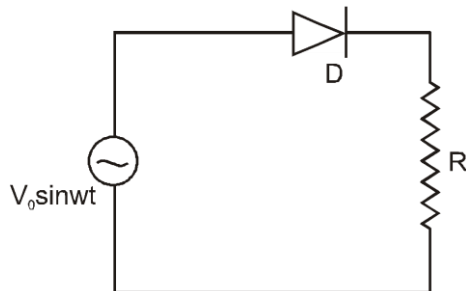
Same as NOR Gate

NOR Gate		
0	0	1
0	1	0
1	0	0
1	1	0

20. For 'OR gate $X = A + B$
 i.e., $0 + 0 = 0$, $0 + 1 = 1$, $1 + 0 = 1$, $1 + 1 = 1$

21. In NOR get $Y = \overline{A+B}$
 i.e., $\overline{0+0} = \overline{0} = 1$, $\overline{1+0} = \overline{1} = 0$
 $\overline{0+1} = \overline{1} = 0$, $\overline{1+1} = \overline{1} = 0$

EXERCISE # 2



5.

$$V_{rms} = \left(\frac{V_0}{2} \right) = \frac{155}{2} = 77.5 \text{ volt}$$

$$V_0 = \frac{310}{2} = 155 \text{ volt.}$$

7. Energy,

$$E_{min} = \frac{hc}{\lambda_{max}} \quad \therefore \quad \lambda_{max} = \frac{hc}{E_{min}}$$

$$= \frac{6.6 \times 10^{-34} \times 3 \times 10^8}{1.43 \times 1.6 \times 10^{-19}} \text{ m} = 8.654 \times 10^{-7} \text{ m}$$

$$= 8654 \times 10^{-10} \text{ m} = 8654 \text{ Å}$$

8. (a) To find the given circuit can be used as an amplifier, we find V_{BE} and V_{CE}

$$V_{BE} = V_{CC} - I_B R_B$$

$$= 5.5 - 10 \times 10^{-6} \times 500 \times 10^3$$

$$= 0.5 \text{ V}$$

$$V_{CE} = V_C - I_C R_C$$

$$= 5.5 - 5.2 \times 10^{-3} \times 1 \times 10^3$$

$$= 0.3 \text{ V}$$

As both the emitter-base junction and collector emitter junction are forward bias (both have positive sign), it can't be used as an amplifier.

(b) In CE configuration,

$$\beta = \frac{I_C}{I_B} = 69 \quad \dots(i)$$

Current gain

$$I_E = I_B + I_C = 7 \text{ mA} \quad \dots(ii)$$

and

From Eqs. (i) and (ii), we get

$$69 = \frac{I_C}{7 - I_C}$$

$$I_C = 6.9 \text{ mA}$$

Substituting the value of I_C in Eq. (ii), we obtain the value of $I_B = 0.1 \text{ mA}$.

EXERCISE # 3 PART - I

1. Only signal having wavelength less than threshold wavelength will be detected.

$$\text{Energy} \quad E = h\nu = h \frac{c}{\lambda}$$

$$\Rightarrow \quad \lambda = \frac{hc}{E}$$

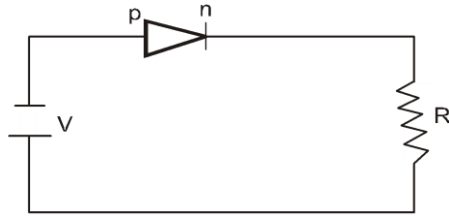
Substituting the value of h , c and E in the above equation

$$\lambda = \frac{6.6 \times 10^{-34} \times 3 \times 10^8}{2.5 \times 1.6 \times 10^{-19}} = 5000 \text{ Å}$$

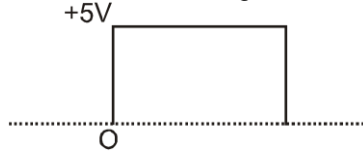
As $4000 \text{ Å} < 5000 \text{ Å}$

Signal of wavelength 4000 Å can be detected by the photodiode

3. (a) In reversed biased p-n junction positive terminal of the battery is connected to the n-side of diode and negative terminal of the battery is connected to p-side of diode.



(b) When input voltage is -5V, the diode is reverse biased and no output is obtained. On the other hand, when input is +5V, the diode is forward biased and output is obtained which is +5V. Therefore, the output wave from is shown in the figure.



(c) The given circuit is a combination of AND and NOT gate (NAND gate). The truth table will be as shown below :

A	B	A.B	$Y = \overline{A.B}$
1	1	1	0
0	1	0	1
1	0	0	1
0	0	0	1

4. In a n-type semiconductors, electrons are majority carriers and holes are minority carriers.

5. The device that can act as a complete circuit is integrated circuit (I.C.).

6. Here,

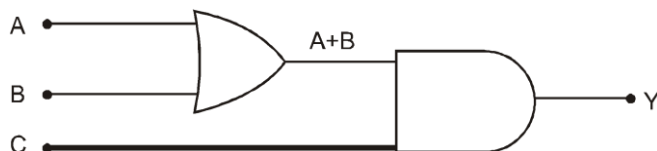
Voltage gain = 50

Input resistance, $R_i = 100\Omega$

Output resistance, $R_o = 200\Omega$

$$\text{Resistance gain} = \frac{R_o}{R_i} = \frac{200\Omega}{100\Omega} = 2$$

$$\text{Power gain} = \frac{(\text{Voltage gain})^2}{\text{Resistance gain}} = \frac{50 \times 50}{2} = 1250$$



7.

The Boolean expression of the given circuit is

$$Y = (A + B) \cdot C$$

The table truth of the given input signals as shown in the table

A	B	C	A + B	$Y = (A + B) \cdot C$
0	1	0	1	0
0	0	1	0	0
1	0	1	1	1
1	0	0	1	0

From the table truth we conclude that output $Y = 1$, for the inputs $A = 1, B = 0, C = 1$

for the inputs $A = 1, B = 0, C = 1$

Hence option (3) is correct

8. It is clear from given logic circuit, that output Y is low when both the inputs are high, otherwise it is high. Thus logic circuit is NAND gate. The truth table of logic gate is

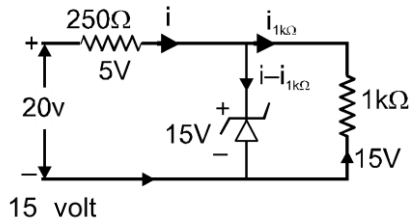
Solids & Semiconductor Devices

A	B	Y
1	1	0
0	0	1
0	1	1
1	0	1

$$y = \overline{A \cdot B}$$

9. Only in (1) and (3)
Diodes are forward biased
As p-type should be higher potential & n-type at lower potential.
10. $n_{i2} = n_e n_h$
 $(1.5 \times 10^{16})^2 = n_e (4.5 \times 10^{22})$
 $n_e = 0.5 \times 10^{10}$
 $n_e = 5 \times 10^9$
 $n_h = 4.5 \times 10^{22}$
 $n_h \gg n_e$
Semiconductor is p-type and $n_e = 5 \times 10^9 \text{ m}^{-3}$.

11. Voltage across zener diode is constant



$$(i)_{1k\Omega} = \frac{1k\Omega}{(20-15)V} = 15 \text{ mA}$$

$$(i)_{250\Omega} = \frac{250\Omega}{250\Omega} = \frac{5V}{250\Omega} = \frac{20}{1000} \text{ A} = 20 \text{ mA}$$

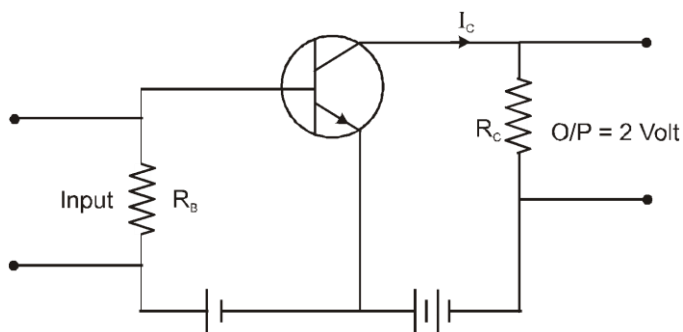
$$\therefore (i)_{\text{zener diode}} = (20 - 15) = 5 \text{ mA.}$$

$$12. \beta = \frac{\Delta I_C}{\Delta I_B} = \frac{10\text{mA}}{200\mu\text{A}} = \frac{10 \times 10^3}{200} = 50$$

15. When small amount of antimony (pentavalent) is added to germanium crystal then crystal becomes n-type semi-conductor.

16. Here D_1 is in forward bias and D_2 is in reverse bias so

$$I = \frac{V}{R} = \frac{5}{10} = \frac{1}{2} \text{ AmP.}$$



$$17. V_O = I_C R_C = 2$$

Solids & Semiconductor Devices

$$I_C = \frac{2}{2 \times 10^3} = 10^{-3} \text{ AmP}$$

$$\text{Current gain} = \frac{I_C}{I_B} = 100$$

$$I_B = \frac{I_C}{100} = \frac{10^{-3}}{100} = 10^{-5} \text{ Amp}$$

$$V_i = R_B I_B = 1 \times 10^3 \times 10^{-5} = 10^{-2} \text{ Volt} \\ = 10 \text{ mV}$$

Ans. (4)

18. ${}^6\text{C} = 1\text{S}_2, 2\text{S}_2, 2\text{P}_2$

${}^{14}\text{Si} = 1\text{S}_2, 2\text{S}_2, 2\text{P}_6, 3\text{S}_2, 3\text{P}_2$

As they are away from Nucleus, so effect of nucleus is low for Si even for Sn and Pb are almost mettalic.

19. $I \rightarrow \text{ON}$

$\text{III} \rightarrow \text{off}$

In II_{nd} state it is uesd as a amplifier it is active reigon.

A	0	1	1	0
B	0	0	1	1
C	1	1	1	1

20.

OR gate

21. Voltage gain = $\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{I_{\text{out}}}{I_{\text{in}}} \times \frac{R_{\text{out}}}{R_{\text{in}}}$

$$= \frac{2 \times 10^{-3}}{40 \times 10^{-6}} \times \frac{4 \times 10^3}{100} = 2 \times 1000 = 2000$$

22. When $A = 1$, $B = 0$, $C = 1$ then $Y = 1$

23. Holes are minority carriers and pentavalent atoms are dopants.

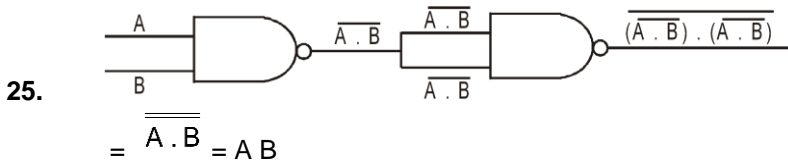
24. $\Delta V = \beta \frac{R_{\text{out}}}{R_{\text{in}}} \Rightarrow G = 25 \frac{R_{\text{out}}}{R_1} \dots\dots\dots(i)$

$$g_m = \frac{\beta}{R_1} \Rightarrow R_1 = \frac{\beta}{g_m} = \frac{25}{0.03}$$

$$G = 25 \frac{R_{\text{out}}}{25} \times 0.03 \dots\dots(i)$$

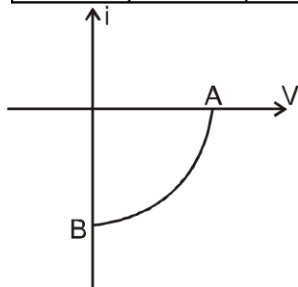
$$G' = 20 \frac{R_{\text{out}}}{20} \times 0.02 \dots\dots(ii)$$

$$G' = \frac{2}{3} G$$



Alternate:

A	B	X
0	0	0
1	0	0
0	1	0
1	1	1



26.

It is $V - i$ characteristic curve for a solar cell, where A represent open circuit voltage of solar cell and B represent short circuit current.

27.

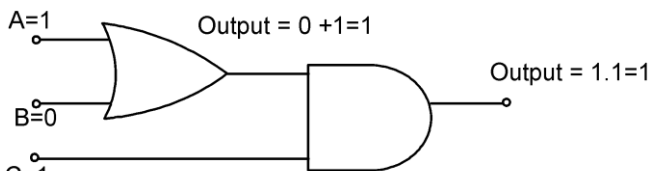
The barrier potential depends on type of semiconductor (for Si $V_b = 0.7$ volt & for Ge $V_b = 0.3$ volt), amount of doping and also on the temperature.

28.

Truth table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

= AND gate (2)



29.

So ans will be (1)

30.

For diode as ideal

$$i = \frac{\Delta V}{R} = \frac{4 - (-6)}{10^3} = 10^{-2} \text{ A}$$

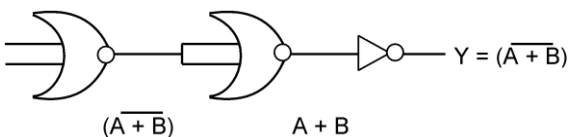
31.

Voltage gain = [current gain] [resistance gain]

$$[.96] \frac{800}{192}$$

Power gain = [current gain] [resistance gain]

$$[.96] [4] = 3.84$$



32.

NOR gate

33.

$$i_c = \frac{3}{3 \times 10^3} \quad A = 10^{-3} \text{ A}$$

Solids & Semiconductor Devices

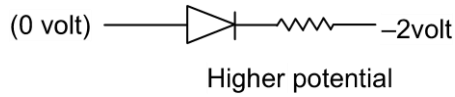
$$i_b = \frac{i_c}{\beta} = 10^{-5} \text{ A}$$

$$R_b = 200 \, \Omega$$

$$V_{in} = R_b i_b = 2 \times 10^{-2} \text{ volt}$$

$$\text{So voltage gain} = \frac{3}{2 \times 10^{-2}} = 150$$

$$\text{Power gain} = 150 \times 100 = 15000$$



34.

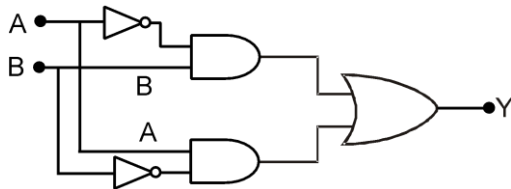
$$i_B = \frac{20 - 0}{500 \times 10^3} = 40 \, \mu\text{A}$$

$$V_{CE} = V_{CC} - i_C R_C$$

$$0 = 20 - (i_C) (4 \times 10^3)$$

$$i_C = \frac{20}{4 \times 10^{-3}} = 5 \text{ mA} \quad \Rightarrow \quad \beta = \frac{i_C}{i_b} = \frac{5 \times 10^{-3}}{40 \times 10^{-6}} = 125$$

36. In p-n junction diode, change in temperature due to heating affect the overall V_f characteristic of a diode



37.

$$y = A\bar{B} + \bar{A}B$$

38. p-type semiconductor holes are majority for creating holes al, ga, B in trivalent impurities are added

39. When switch A \rightarrow on LED light up

A	B	output
1	0	1

so when switch B is switch on A is off then Led light up

A	B	output
0	1	0

When switch of A and B both on short circuit full current flous through switch led \rightarrow switch off

A	B	output
1	1	0

$$40. \quad \Delta E = \frac{hc}{\lambda} \quad \Rightarrow \quad \lambda = \frac{hc}{E} = \frac{1240 \text{ eV nm}}{1.9 \text{ eV}} = 654 \text{ nm}$$

A	B	Out put
0	0	1
0	1	0
1	0	0
1	1	0

41.

Since the truth table is similar to NOR gate, so this system will behave like a NOR gate

PART - II

1. The output voltage is given by,

$$V_0 = V_i \times \beta \times \frac{R_L}{R_{BE}}$$

Here, $V_i = 1 \text{ mV}$, $\beta = 100$

$R_L = 10 \text{ k}\Omega$, $R_{BE} = 1 \text{ k}\Omega$

$$\therefore V_0 = 1 \times 10^{-3} \times 100 \times \frac{10}{1} = 1.0 \text{ V}$$

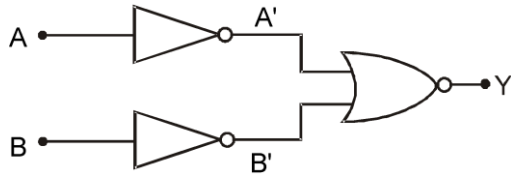
2. The resistivity of semiconductor decreases with increase in temperature and is given by

$$\rho_T = \rho_0 e^{E_g/k_B T}$$

Where E_g is the energy gap, k_B is the Boltzmann constant, T is the absolute temperature.

3.

Truth table



A	B	A'	B'	Y
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

Output of this is same as that of AND gate. Alternatively
The Boolean expression for the given logic gate is

$$Y = \overline{A + B}$$

Applying De Morgan's theorem $Y = \overline{A} \cdot \overline{B} = A \cdot B$

This is the Boolean expression for the AND gate.

4.

Voltage gain,

$$A_v = \beta \times \frac{R_0}{R_i} = 50 \times \frac{5}{1} = 250$$

PART - III

1.

$$Y = (\overline{A + B}) = A \cdot B$$

it is AND gate.

2.

From Half wave rectifier

3.

$$(\overline{A + B}) = \text{NOR gate}$$

When both inputs of NAND gate are connected, it behaves as NOT gate OR + NOT = NOR.

4.

$$\begin{aligned}
 y &= \left(\overline{A \cdot A \cdot B} \right) \cdot \left(\overline{B \cdot A \cdot B} \right) \\
 &= \left(\overline{A \cdot A \cdot B} \right) \cdot \left(\overline{B \cdot A \cdot B} \right) \\
 &= A \cdot (\overline{A + B}) + B \cdot (\overline{A + B}) \\
 &= A \cdot \overline{A} + A \cdot \overline{B} + B \cdot \overline{A} + B \cdot \overline{B} \\
 y &= 0 + A \cdot \overline{B} + B \cdot \overline{A} + 0
 \end{aligned}$$

5.

For forward bias $V_P > V_N$

So is forward biased.

6.

For conductor (Cu) resistance increases linearly and for semiconductor resistance decreases exponentially in given temperature range.

7.

Whenever we have 1 at input, output is 1.
So the gate is or

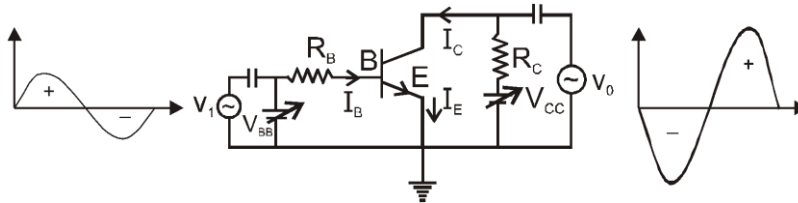
8.

From standard data
Ans. is (4)

9.

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\alpha = \frac{\beta}{\beta + 1}$$



10.

$$\Delta V_{CC} = \Delta V_{CE} + R_L \Delta I_C = 0$$

$$\text{or } \Delta V_{CE} = -R_L \Delta I_C$$

The change in V_{CE} is the output voltage v_0 . From equation we get

$$v_0 = \Delta V_{CE} = -\beta_{ac} R_L \Delta I_B$$

The voltage gain of the amplifier is

$$A_v = \frac{v_0}{v_i} = \frac{\Delta V_{CE}}{r \Delta I_B} = -\frac{\beta_{ac} R_L}{r}$$

The negative sign represents that output voltage is opposite with phase with the input voltage.

11. For silicon diode barrier potential is 0.7V

$$\frac{3 - 0.7}{200}$$

$$\text{So } I = \frac{3 - 0.7}{200} = 0.0115 \text{ A} = 11.5 \text{ mA}$$

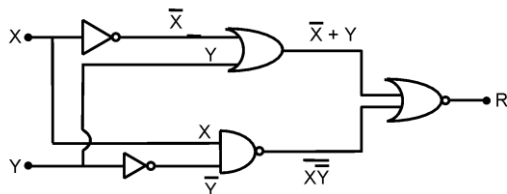
12. $\sigma = ne\mu$

$$\rho = \frac{1}{ne\mu} = \frac{1}{10^{19} \times 1.6 \times 10^{-19} \times 1.6} = \frac{1}{2.56} \approx 0.4 \Omega \text{ m}$$

13. For shown case $V_0 = 12 - 0.3 = 11.7$

In second case $V_0 = 12 - 0.7 = 11.3$

So difference = 0.4 V

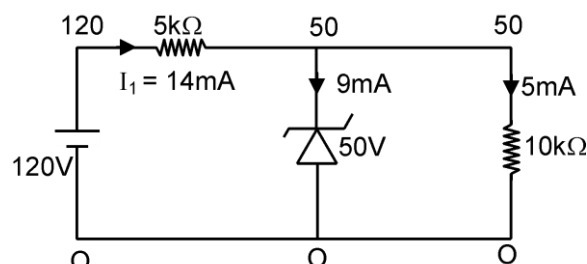


14.

$$R = \overline{(\overline{X + Y}) + \overline{XY}} = \overline{(\overline{X + Y})} \overline{\overline{XY}} = (\overline{\overline{X + Y}}) \cdot \overline{\overline{XY}} = (X + Y) \cdot (XY) = (XY)(XY)$$

$$\therefore R = XY$$

$$X = 1, Y = 0$$

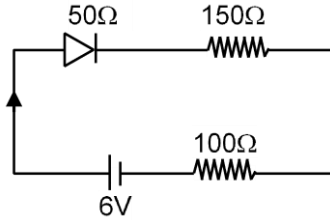


15.

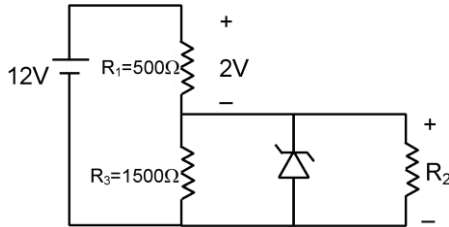
$$I = 9 \text{ mA}$$

Solids & Semiconductor Devices

16. Since the second diode is reverse biased the simplified circuit is as shown in the figure



$$I = \frac{6}{300} = 0.02 \text{ A}$$



- 17.

If we consider break down in zener diode, then potential across R_3 will be 10V and R_1 will be 2V.

So current in R_3 will be $i_3 = \frac{10}{1500} = \frac{2}{300} \text{ A}$

and current in R_1 will be $i_1 = \frac{2}{500} \text{ A}$

$\Rightarrow i_1 < i_3$, which is not possible

\Rightarrow Potential difference across zener diode does not reach to break down voltage. So no current will flow through reverse biased zener diode.

18. When switched on,

$$V_{CE} = 0$$

$$V_{CC} - R_C i_C = 0$$

$$i_C = \frac{V_{CC}}{R_C} = \frac{5}{1 \times 10^3} = 5 \times 10^{-3} \text{ A}$$

$$i_C = \beta i_B$$

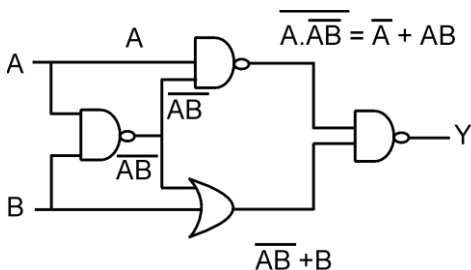
$$i_B = \frac{i_C}{\beta} = \frac{5 \times 10^{-3}}{200} = 25 \times 10^{-6} \text{ A} = 25 \mu\text{A}$$

Using KVL at input side,

$$V_{BB} - i_B R_B - V_{BE} = 0$$

$$V_{BB} = V_{BE} + i_B R_B$$

$$= 1 + 100 \times 10^3 \times 25 \times 10^{-6} = 1 + 2.5 = 3.5 \text{ V}$$



- 19.

$$Y = \overline{A.AB} \cdot (\overline{AB} + B)$$

$$Y = \overline{A.AB} + \overline{AB} + B$$

$$= A.AB + AB.B$$

$$\begin{aligned} &= A(\overline{A} + \overline{B}) + (AB)\overline{B} \\ &= A\overline{B} + 0 \end{aligned}$$